

Welcome to IEEE Xplore<sup>®</sup>

- Home
- What Can I Access?
- Log-out

## Tables of Contents

- Journals & Magazines
- Conference Proceedings
- Standards

## Search

- By Author
- Basic
- Advanced

## Member Services

- Join IEEE
- Establish IEEE Web Account
- Access the IEEE Member Digital Library

Your search matched **4** of **943290** documents.

A maximum of **4** results are displayed, **25** to a page, sorted by **Relevance** in **descending** order.  
 You may refine your search by editing the current search expression or entering a new one the text box.  
 Then click **Search Again**.

*extract\* and timing and model*

## Results:

Journal or Magazine = **JNL** Conference = **CNF** Standard = **STD****1 Timing model extraction of hierarchical blocks by graph reduction***Moon, C.W.; Kriplani, H.; Belkhale, K.P.;*

Design Automation Conference, 2002. Proceedings. 39th , 10-14 June 2002

Page(s): 152 -157

[\[Abstract\]](#) [\[PDF Full-Text \(646 KB\)\]](#) **IEEE CNF****2 Automated analysis of timing faults in synchronous MOS circuits***Vanden Meersch, E.; Claesen, L.; De Man, H.;*

Circuits and Systems, 1988., IEEE International Symposium on , 7-9 June 1988

Page(s): 487 -490 vol.1

[\[Abstract\]](#) [\[PDF Full-Text \(324 KB\)\]](#) **IEEE CNF****3 General experimental method of parameter extraction for CMOS timing macromodels***Wu, C.-Y.; Jang, W.-Y.; Wu, H.-J.;*

Communications, Speech and Vision, IEE Proceedings I [see also IEE Proceedings- Communications] , Volume: 135 Issue: 2 , April 1988

Page(s): 39 -47

[\[Abstract\]](#) [\[PDF Full-Text \(688 KB\)\]](#) **IEE JNL****4 High-level circuit modeling for power estimation***Schimpfle, C.V.; Simon, S.; Nossek, J.A.;*

Electronics, Circuits and Systems, 1999. Proceedings of ICECS '99. The 6th IEEE International Conference on , Volume: 2 , 5-8 Sept. 1999

Page(s): 807 -810 vol.2